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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,363	MCDERMOTT ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-180* is/are pending in the application.

4a) Of the above claim(s) *1-90 and 180* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *91-179* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: Attaching papers of "DECISION TO ACCEPT COLOR DRAWINGS" and conversion .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 92, 93 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 92 is unclear because since as claimed in claim 91, the applicant recited the cavity, which is a removal portion of the dielectric material being an obtuse (the angle is in a range of $90<x<180$, x is an obtuse angle), so it has to be greater than 60 degrees, so what does applicant means in claim 92?

Please, clarify.

Claim 93 is unclear because since claim 91 already recited "the conductive layer built up on the dielectric material to form teeth." Does applicant mean the teeth in claim 91 are the same or different the teeth in claim 93?

Please, clarify.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 97-110, 112-119, 122-179 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura (U.S. Patent 5,517,758).

As to claim 97, Nakamura discloses an electrical device as shown in figures 1-9 including:

a dielectric material (2) having cavities (3) remaining from removal of a portion (1) of the dielectric material (2),

a conductive layer (4) built up on the dielectric material (2) to fill the cavities (3) to form a surface of substantially angular teeth set in the dielectric material (2), and wherein the conductive layer (4) is a portion of circuitry (element 77 of figure 7) of the electrical device, and a sample of the circuitry having at least 20% of the teeth being at least 0.1 mil deep, see figure 1D shows the insulation layer 2 having cavities with at least 0.1 mil and the roughness surface of the conductive layer 4 contact/connect and fit to the roughness surface of the insulating layer 2, so the deep of the surface of the conductive layer 4 having at least 0.1 mil in deep.

As to claim 98, Nakamura discloses the removal of the portion (1) as shown in figure (1) is sufficient to produce a surface gloss measurement at an angle of 60 degrees of less than 10%, it can be seem from figure (1) that the opening (3) having an angle, which is approximately 60 degrees.

As to claim 99, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) has a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass

roughening (the figure 1D contains the conductive layer 4 having a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass roughening comparing of the Prior art of figure 2 in the application).

As to claim 100, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) filled in the cavities (3) sufficient for a peel strength greater than a peel strength that would be produced by a single desmear process, see table 1, column 6.

As to claim 102, Nakamura discloses an electrical device as shown in figures 1-9 including:

a conductive layer (4) of material built up on a layer of a dielectric material (2), the layers (4, 2) joined in a saw-tooth manner (see figure 1) made of both materials in an interlocking bite; wherein the conductive layer (4) is a portion of circuitry of the electrical device, the conductive layer (4) comprised of teeth, and a sample of circuitry having at least 5,000 of the teeth per linear inch.

Note: 1 inch = 2.54 cm = 1000 mil, and 1 cm = 0.3937 inch (~0.4 in), so 5 mu ~ 0.19 mil; therefore, in one inch the roughness surface having at least 1000*10*2.54 or ~ to 25,400 samples per linear inch

As to claims 101, 107, Nakamura discloses the conductive layer (4) is built up in the cavities (3) sufficiently that separation would destroy integrity of the portion of the dielectric material.

As to claim 105, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) has a dielectric surface contact area

greater than a dielectric surface contact area that would be produced by a single pass roughening (the figure 1D contains the conductive layer 4 having a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass roughening comparing of the Prior art of figure 2 in the application).

As to claim 106, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) filled in the cavities (3) sufficient for a peel strength greater than a peel strength that would be produced by a single desmear process, see table 1, column 6.

As to claim 103, Nakamura discloses the electrical device comprised a micro via (tooth or cavity of the dielectric material).

As to claim 104, Nakamura discloses the removal of the portion (1) as shown in figure (1) is sufficient to produce a surface gloss measurement at an angle of 60 degrees of less than 10%, it can be seem from figure (1) that the opening (3) having an angle, which is approximately 60 degrees.

Note: 1 inch = 2.54 cm = 1000 mil, and 1 cm = 0.3937 inch (~0.4 in), so 5 mu ~ 0.19 mil; therefore, in one inch the roughness surface having at least 1000*10*2.54 or ~ to 25,400 samples per linear inch.

As to claim 110, Nakamura discloses an electrical device as shown in figures 1-9 including a dielectric material (2) with cavities (3) remaining after removal of a portion (1) of the dielectric material sufficient to produce a surface gloss measurement at an angle of 60 degrees of less than 10%, see figure 1, and electrical device circuitry comprised of a conductive layer (4) built up to fill the cavities.

As to claim 115, Nakamura discloses an electrical device as shown in figures 1-9 including: a dielectric material (2), and electrical device circuitry comprising a conductive layer (4) built up on the dielectric material (2) at a dielectric surface area greater than a dielectric surface area that would be produced by a single pass roughening (the figure 1D contains the conductive layer 4 having a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass roughening comparing of the Prior art of figure 2 in the application), and a sample of circuitry having at least 20% of the teeth that are within the range of 0.1-0.2 mil deep, see table 1.

As to claims 112-113, 117, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) filled in the cavities (3) sufficient for a peel strength greater than a peel strength that would be produced by a single desmear process, see table 1, column 6.

As to claim 114, 118, Nakamura discloses the conductive layer (4) is built up in the cavities (3) sufficiently that separation destroy integrity of the portion of the dielectric material.

As to claim 116, Nakamura discloses the electrical device comprised a micro via (tooth or cavity of the dielectric material).

As to claim 119, Nakamura discloses an electrical device as shown in figures 1-9 including a dielectric material (2), a conductive layer (4) forming a portion of circuitry of the electrical device, and means for joining the conductive layer (4) to the dielectric material (2), the means including teeth built up on the dielectric material and angled sufficiently (see figure 1).

As to claims 122-123, Nakamura discloses an electrical device comprising a circuit board as shown in figures 1-9 including a dielectric material (2), and electrical device circuitry comprising a conductive layer (4) built up on a surface of the dielectric material to produce a peel strength greater than a peel strength that would be produced by a single desmear process, see table 1, and a sample of circuitry having at least 20% of the teeth that are within the range of 0.1-0.2 mil deep, see table 1.

As to claim 124, Nakamura discloses the conductive layer (4) is built up in the cavities (3) sufficiently that separation destroy integrity of the portion of the dielectric material.

As to claims 125-126, Nakamura discloses an electrical device as shown in figures 1-9 including a dielectric material (2) having a top surface with a surface remaining from removal of a portion (1) of the dielectric material, and means for mechanically gripping (comprised of teeth) a conductive layer (4) to the surface of the dielectric material (2) so that the conductive layer is burrowed in and under the top surface of the dielectric material, wherein the conductive layer (4) forms a portion of circuitry of the electrical device.

As to claims 127-128, Nakamura discloses an electrical device as shown in figures 1-9 including a dielectric material (2), and electrical device circuitry comprising a conductive layer (4) comprised of teeth built up on the dielectric material sufficiently that separation would requires destroying integrity of the portion of the dielectric material.

As to claims 129-130, Nakamura discloses an electrical device as shown in figures 1-9 including: a dielectric material (2) having a surface gloss measurement at an

angle of 60 degrees of less than 10%; and circuitry of the electrical device comprised of a conductive layer (4) comprised of teeth on the dielectric material (2).

As to claims 131-133, Nakamura discloses the conductive layer (4) is built up in the cavities (3) sufficiently that separation would destroy integrity of the conductive layer and or the dielectric material.

As to claims 134-135, Nakamura discloses an electrical device as shown in figures 1-9 including a dielectric material (2), and means for joining a conductive layer (comprised of teeth) (4) built up on the dielectric material (2) at a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass roughening the figure 1D contains the conductive layer (4) having a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass roughening comparing of the Prior art of figure 2 in the application), wherein the conductive layer is a portion of circuitry of the electrical device.

As to claims 136-137, Nakamura discloses an electrical device as shown in figures 1-9 including a dielectric material (2), and means for joining a conductive layer (4) built up on the dielectric material sufficiently that separation requires destroying integrity of a portion of the dielectric material, said means for joining comprising filled cavities (3) that form a portion of circuitry of the electrical device, the filled cavities comprised of teeth.

Regarding claims 138-143, Nakamura discloses a sample of the circuitry having at least 5,000-15,000 teeth per linear inch or 25,000-200,000 teeth per square inch, see claim 102.

As to claims 144-145, Nakamura discloses a sample of the circuitry having at least 20% of the teeth having a shape that mechanically grips the dielectric layer (2), and 50% of the teeth that are obtuse shaped.

As to claims 152-157, Nakamura discloses the device in figures 7-9 the circuitry of the electrical device is comprised of multi-layer circuitry, one of said multi-layers having said teeth and another of said layers having corresponding teeth

As to claims 158-159, Nakamura discloses the device in figures 7-9 the circuitry of the electrical device is comprised of multi-layer circuitry, one of said multi-layers having said teeth and another of said layers having corresponding teeth.

As to claims 166-171, Nakamura discloses the device as shown in figures 7-9 the circuitry is comprised of double sided circuitry, one side having said teeth and another side having corresponding teeth (top and bottom surface having teeth).

As to claims 172-173, Nakamura discloses the device as shown in figures 7-9 the circuitry is comprised of double sided circuitry, one side having said teeth and another side having corresponding teeth (top and bottom surface having teeth).

Regarding claims 146-151, Nakamura discloses a sample of the circuit board has at least 20% or 50% of the teeth are within the range of at least 0.1-0.2 mil deep.

As to claims 160-165, Nakamura discloses the device in figures 7-9 the circuitry of the electrical device is comprised of multi-layer circuitry, one of said multi-layers having said teeth and another of said layers having corresponding teeth.

As to claims 174-179, Nakamura discloses the device as shown in figures 7-9 the circuitry is comprised of double sided circuitry, one side having said teeth and another side having corresponding teeth (top and bottom surface having teeth).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 91-96, 108-109, 111, 120-121, and 138-179 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (U.S. Patent 5,517,758) in view of Katagiri et al. (U.S. Patent 5,158,827).

As to claims 91-93, 108-109, Nakamura discloses an electrical device as shown in figures 1-9 including:

a dielectric material (2, column 4, line 57, column 5, lines 39-40) having a top surface with cavities or undercuttings (3, see figure 1C) remaining from removal of a portion (1) of the dielectric material (2),

a conductive layer (4, column 6, line 52) built up on the dielectric material (2) to filled the cavities (3) to form teeth set in and under the top surface of the dielectric material, and

wherein the conductive layer (4) is a portion of circuitry (or element 77 of figure 7E) of the electrical device.

Nakamura does disclose the cavities each being at least 0.1 mil deep (***note: the term at least 0.1 mil is equivalent to greater than or equal to 0.1mil or such in a range of [0.1,infinity, so in Nakamura's table 1 shows the roughness surface in a range of (5-12 micrometters, which is equivalent to 0.19685mil***).

Nakamura does not specific disclose an angle of the cavity being obtuse (>90 but less than 180 degrees)

Katagiri et al. shows a circuit board as shown in figures 1-3 comprising a matt film (dielectric material) (2, column 3, line 38) having cavities each being obtuse see figures 1-2.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a circuit board having a roughness surface having cavities each having an obtuse angle as taught by Katagiri modified the dielectric material of Nakamura in order to provide an easy and excellent bonding surface.

As to claim 94, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) has a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass roughening (the figure 1D contains the conductive layer 4 having a dielectric surface contact area greater than a dielectric surface contact area that would be produced by a single pass roughening comparing of the Prior art of figure 2 in the application).

As to claim 95, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) filled in the cavities (3) sufficient for a peel

strength greater than a peel strength that would be produced by a single desmear process, see table 1, column 6.

As to claim 96, Nakamura discloses the removal portion does not include a physical roughening, and conductive layer (4) filled in the cavities (3) sufficient for a peel strength greater than a peel strength that would be produced by a single desmear process, see table 1, column 6.

Regarding claim 111, Nakamura does not specific disclose an angle of the cavity being obtuse (>90 but less than 180 degrees)

Katagiri et al. shows a circuit board as shown in figures 1-3 comprising a matt film (dielectric material) (2, column 3, line 38) having cavities each being obtuse see figures 1-2.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a circuit board having a roughness surface having cavities each having an obtuse angle as taught by Katagiri modified the dielectric material of Nakamura in order to provide an easy and excellent bonding surface.

As to claims 120-121, Nakamura discloses an electrical device as shown in figures 1-9 including a dielectric material (2); and means for joining (comprised of teeth, which is cavities) a conductive layer (4) built up on the dielectric material to produce a peel strength greater than a peel strength that would be produced by a single desmear process, see table 1, column 6, wherein the conductive layer is a portion of circuitry, and the dielectric material having at least 0.1 mil in deep, see table 1.

Nakamura does not specific disclose the dielectric material having an angle of the cavity being obtuse (>90 but less than 180 degrees)

Katagiri et al. shows a circuit board as shown in figures 1-3 comprising a matt film (dielectric material) (2, column 3, line 38) having cavities each being obtuse see figures 1-2.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a circuit board having a roughness surface having cavities each having an obtuse angle as taught by Katagiri modified the dielectric material of Nakamura in order to provide an easy and excellent bonding surface.

Regarding claims 138-143, Nakamura discloses a sample of the circuitry having at least 5,000-15,000 teeth per linear inch or 25,000-200,000 teeth per square inch, see claim 102.

As to claims 144-145, Nakamura discloses a sample of the circuitry having at least 20% of the teeth having a shape that mechanically grips the dielectric layer (2), and 50% of the teeth that are obtuse shaped.

As to claims 152-157, Nakamura discloses the device in figures 7-9 the circuitry of the electrical device is comprised of multi-layer circuitry, one of said multi-layers having said teeth and another of said layers having corresponding teeth

As to claims 158-159, Nakamura discloses the device in figures 7-9 the circuitry of the electrical device is comprised of multi-layer circuitry, one of said multi-layers having said teeth and another of said layers having corresponding teeth.

As to claims 166-171, Nakamura discloses the device as shown in figures 7-9 the circuitry is comprised of double sided circuitry, one side having said teeth and another side having corresponding teeth (top and bottom surface having teeth).

As to claims 172-173, Nakamura discloses the device as shown in figures 7-9 the circuitry is comprised of double sided circuitry, one side having said teeth and another side having corresponding teeth (top and bottom surface having teeth).

Regarding claims 146-151, Nakamura discloses a sample of the circuit board has at least 20% or 50% of the teeth are within the range of at least 0.1-0.2 mil deep.

As to claims 160-165, Nakamura discloses the device in figures 7-9 the circuitry of the electrical device is comprised of multi-layer circuitry, one of said multi-layers having said teeth and another of said layers having corresponding teeth.

As to claims 174-179, Nakamura discloses the device as shown in figures 7-9 the circuitry is comprised of double sided circuitry, one side having said teeth and another side having corresponding teeth (top and bottom surface having teeth).

Response to Arguments

Applicant's arguments with respect to claims 91-179 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
August 15, 2006.